USB ENGINEERING CHANGE NOTICE

Title: HSIC ECN
Applies to: High Speed Inter Chip Specification, Rev 1.0

Summary of ECN:

This ECN changes the HSIC electrical specification parameters concerning:

- Total Capactive load replaced with a combination of input buffer load (1 pf -5 pf) and trace length (2cm -10cm) parameters
- Slew Rate(TSLEW) range changed to 0.7 V/ns to 2 V/ns
- Weak Keepers specifyied as pullup/pulldown keeper resistors (RK) with a range as 17KΩ to 60KΩ
- Receiver Data Setup (TS) value changed to 365 ps from 300 ps and a new transmitter uncertainty (TT) parameter specified at 365 ps

The ECN also clarifies the HSIC protocol specification concerning:

- CONNECT is required to be signaled (STROBE line low, DATA line high) for a *minimum* 2 strobe periods
- Timing for when bus keepers must be enabled or disabled when entering or exiting idle conditions.

The ECN also includes supplemental information on the receiver implementation for data signaling:

- An adaptive receiver recommendation is made to ensure backwards compatibility with any existing legacy HSIC devices

Reasons for ECN:

The current HSIC Electrical Specification does not accurately reflect measured system data. Correcting this mismatch will ensure interoperability between devices. For example;

- The modified capacitive Loading model ensures that driver circuits are accurately designed to meet the specified loads for different temperature corners.
- The modified Slew rate parameters ensure values are fast enough to allow receivers to be accurately designed for compliance.
- The modified slew rate values ensure margin for crosstalk and impedance mismatch.
- The modified bus keeper parameters clarifies the specification

The clarifications made to the HSIC Protocol specification will improve the relevant documentation in the HSIC specification and will ensure inter-operability of devices.

The supplemental information on Data Signaling clarify the HSIC specification and ensures data encoding parity with the USB Specification revision 2.0. Additionally, it ensures that data generated on an HSIC interface is encoded in a compatible format to traditional HS USB data for high-speed repeater path transfers internal to USB hubs.

Impact on existing peripherals and systems:

- HSIC devices that have already been designed will not be affected since they will be compliant with the ECN modifications.
- The proposed spec changes will help simplify future implementations of HSIC PHYs

- The impact should be zero. This is a clarification which will ensure interoperation with existing USB HS signaling and HS hubs. There are no known existing HSIC receivers that are designed to filter HSIC packets that transmit data using inverted encoding. The reason for this is that the UTMI specification defines an identical encoding, and that has been used by all known HSIC receiver implementations

Hardware Implications:

- HSIC devices that have already been designed will not be affected since they will be compliant with the ECN modifications.
- The proposed spec changes will help simplify future implementations of HSIC PHYs
- All known existing designs already comply.

Software Implications:

None

Compliance Testing Implications:

None

Specification Changes:

1 Electrical Spec Changes

1.1 Total Capacitive Load:

Current Spec:
Page 16, Section 4 of the spec lists a table that specifies:

- Total Capacitive Load (CL) range as 3 pf to 14 pf.
- Circuit Board Trace Length (TL) range maximum at 10 cm

Change:
Modify the table in Page 16, Section 4 of the spec as below:

- Replace the row specifying the Total Capacitive Load (CL) range with a row specifying the Input Buffer Load (BL) range as 1 pf to 5 pf
- Circuit Board Trace Length (TL) range as 2 cm to 10 cm

Reason: Current specified values do not accurately reflect actual systems. For actual systems the connection is a transmission line and the distributed capacitance must not be included as a lumped load. A realistic input buffer load range is 1-5 pf. The minimum trace length specified will allow slew rates to be tuned for a minimum load of 3pf (1 pf load + 2pf trace)

1.2 Slew Rate (Rise and Fall) Strobe and Data

Current Spec:
Page 16, Section 4 of the spec lists a table that specifies:

- Slew Rate (TSLEW) range as 0.6*Vdd to 1.2 V/ns

Change:
Modify the table in Page 16, Section 4 of the spec as below:

- Specify the Slew Rate(TSLEW) range as 0.7 V/ns to 2 V/ns depending on the operating process-voltage-temperature condition.

Reason: Current specified values are too slow and do not allow any margin for crosstalk and impedance mismatch.

1.3 Bus Keeper

Current Spec:
Page 16, Section 4 of the spec lists a table that specifies:

- I/O Weak Keepers (IL) range as 20 to 70uA

Change:
Modify the table in Page 16, Section 4 of the spec as below:

- Replace the I/O Weak Keepers (IL) row with a row specifying the pullup/pulldown keeper resistor (RK) with a range as 17KΩ to 60KΩ

Reason: It is not clear how the current specified current is measured. If this parameter is to be defined as a current there should be a V/I characteristics chart so the designer knows that is keeper behavior is the expected in all conditions. Proposed solution converts existing specified current range based on ohms law.

1.4 HSIC receiver – Setup Time

Current Spec:
Page 16, Section 4 of the spec lists a table that specifies:

- Receiver Data Setup (TS) value at 300 ps

Change:
Modify the table in Page 16, Section 4 of the spec as below:

- Receiver Data Setup (TS) value at 365 ps
- Add a row that specifies the transmitter uncertainty (TT) at 365 ps

Reason: At the transmitter side several design restrictions can be avoided if the current 300ps value is increased. This proposal calls for dividing the setup budget (1.042 ns) in the following manner: 35% for the receiver, 35% for the transmitter and 30% for the board. (0.35 * 1.042ps = 365ps)

2 Protocol Changes

2.1 Connect Signaling

Current Spec:
Section 3.3 of the specification states - “CONNECT (STROBE line low, DATA line high) for 2 strobe eriods” - that the connect signaling corresponds to Strobe line low and Data line high for 2 Strobe-periods with no tolerance defined

Change: Replace text in Section 3.3 with ““CONNECT (STROBE line low, DATA line high) for a minimum 2 strobe periods”. This change clarifies that the peripheral must send the connect signaling for a minimum of 2 strobe periods. The host must detect the connect signaling if seen for a minimum of 1 Strobe-period.

Reason: Overall intention of the spec is that the CONNECT detection would typically be implemented as a debounced edge detection (not a timed event), and since 1 STROBE period is adequate for the detection on the receiver side (whether it is edge detected or a timed event), the driver side was defined to be 2 STROBE periods to ensure that a minimum of 1 STROBE period was available to the receiver under all conditions. The change helps clarify the intent of the spec.

2.2 Bus Keeper Timing

Current Spec:
Section 3.5 of the spec states “ These keepers must be disabled 1 Strobe-period after any non-IDLE bus state is detected, and must be enabled 1 Strobe-period after IDLE is detected.”

Change:
Modify Section 3.5 of the spec as such – ““ These keepers must be disabled 1.5 Strobe-periods (with a tolerance of +/- 0,5 Strobe-periods) after any non-IDLE bus state is detected, and must be enabled 1.5 Strobe-periods (with a tolerance of +/- 0,5 Strobe-periods) after IDLE is detected”

Reason: This change will make a pure digital logic implementation much easier and straight-forward to implement with a very small increase of power consumption.

3 Data Signaling Text Additions

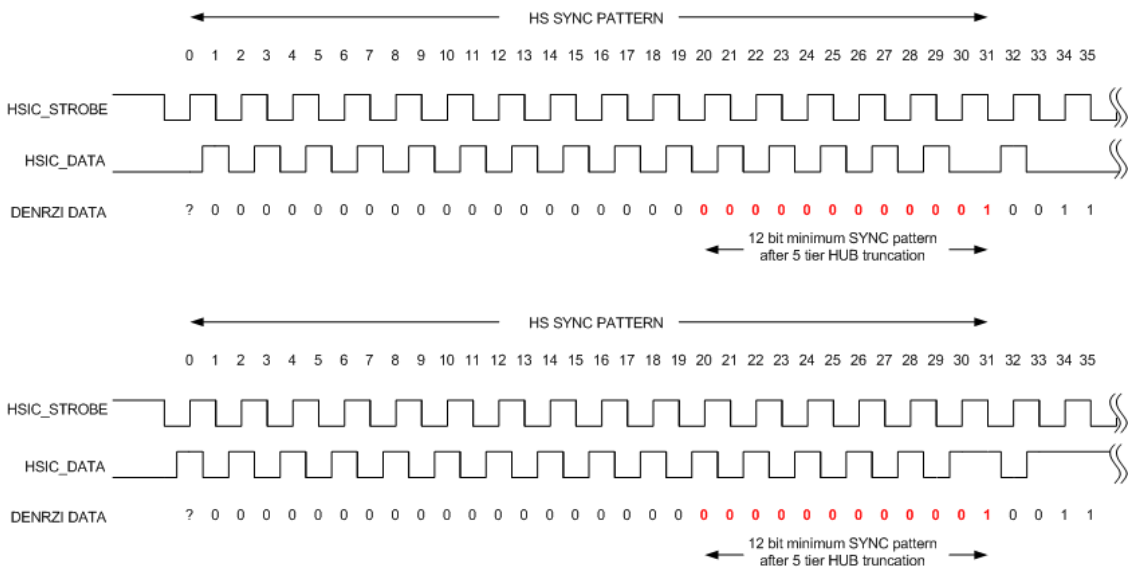
The following text additions to the High Speed Inter Chip Specification, section 3.4 Data Signaling:(the existing text in section 3.4 remains, the text below is added as supplemental information after the existing text)

The HSIC receiver should be designed to be adaptive, meaning that the HSIC receiver does not filter packets based on a USB “J” or USB “K” encoding, but instead uses the decoded NRZI (DENZRI) and unstuffed data (the raw data). Please see the example below showing SYNC packet encoding and inverted encoding, and how the raw data is identical.

Additionally, the HSIC transmitter should be designed to transmit packets as defined in the USB specification with the following encoding association. A logic ‘1’ state on the HSIC interface is equivalent to a high-speed (HS) USB ‘J’. A logic ‘0’ state on the HSIC interface is equivalent to a high-speed (HS) USB ‘K’.

When the HSIC interface is included as part of a hub and is connected to a high-speed hub repeater path, the repeater path data will be transmitted with the encoding that is on the repeater path.

Example: The first pattern is an HSIC data pattern of (0101…0100). The second SYNC pattern is (1010…1011), the inverse of the previous pattern. In both cases the resulting raw data (DENRZI) is identical (0000…0001) which is a valid USB SYNC in both cases.



Reason: The adaptive receiver recommendation is that many USB PHYs are designed to qualify USB packets based on the DENRZI unstuffed data and the encoded repeater path data may not meet the above listed encoding requirements. Additionally, this will ensure that receivers maintain backward compatibility with any existing legacy HSIC devices that may transmit inverted data